22. (Amended) The system of claim 21, wherein the digital signal processor further comprises a software program which, upon execution, causes the system to:

   identify a stage of a trellis diagram;

   identify a number of nodes in the stage; and

   identify a number of branches extending from each node.

25. (Amended) The system of claim 24, wherein the butterfly coprocessor is coupled to compute path metrics for the stage.

26. (Amended) The system of claim 25, wherein the butterfly units are coupled to simultaneously compute a path metric for each node of the stage.

Remarks:

A.   Rejection of Claim 10 Under 35 U.S.C. § 112

The Office Action has rejected pending claim 10 under 35 U.S.C. § 112 second paragraph as being indefinite. Claim 10 has been amended to recite that the butterfly coprocessor units perform approximations of logarithmic sum exponential operations. Accordingly, it is respectfully submitted that rejection to claim 10 is overcome.

B.   Rejection of Claims Under 35 U.S.C. § 102

Pending claims 1-9, 11-14, 17-21, 23, 25 and 26 stand rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,742,621 (Amon). Applicant respectfully traverses the rejection. With respect to claims 1 and 21, Amon does not disclose "a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor". In

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this regard, the Office Action states that the digital signal processor of Amon is all of data processing system 20 shown in FIG. 1 of Amon. Office Action, p. 3. As such, the program control unit 46 of Amon (contended by the Office Action to be the "butterfly processor") is part of the digital signal processor and is thus not coupled thereto as recited by claims 1 and 21. For at least this reason, claim 1 and claims 2-9 and 11-12 depending therefrom and claim 21 and claims 23, 25, and 26 depending therefrom are patentable over Amon.

With respect to claims 13 and 19, nowhere does Amon disclose "simultaneously computing two or more path metrics for the stage based upon the branch metrics." In this regard Applicant respectfully disagrees that Amon "teaches simultaneously computing two or more path metrics (PM1 and PM2) based upon the branch metrics (blocks 101-103) in Figure 3." Office Action, p. 5. Instead, in Amon the path metrics are not simultaneously computed, as the path metrics are computed at different steps and at different times. For at least this reason, claim 13 and claim 14 depending therefrom and claim 19 and claim 20 depending therefrom are patentable over Amon.

For similar reasons, claim 17 is patentable over Amon, as nowhere does Amon disclose simultaneously calculating new path metrics for each node of a stage of a trellis diagram. Thus for at least this reason, claim 17 and claim 18 depending therefrom are patentable over Amon.

C.   **Rejection of Claims Under 35 U.S.C. § 103(a)**

Claims 15, 16, 22 and 24 stand rejected under 35 U.S.C. § 103(a) over Amon in view of U.S. Patent No. 5,796,757 (Czaja). Applicant respectfully traverses the rejection. As discussed above, Amon does not teach or suggest simultaneously computing two or more path metrics. Nor does Czaja. Accordingly, claims
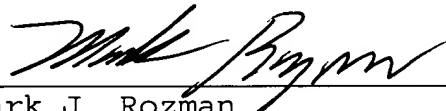
15 and 16 which depend from claim 13 are patentable over the proposed combination.

With regard to claims 22 and 24, neither Amon nor Czaja teach or suggest a butterfly coprocessor coupled to a digital signal processor to perform an operation scheduled by the digital signal processor. Accordingly, claims 22 and 24 depending from claim 21 are patentable over the proposed combination.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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1   1.   A system comprising:

2   a   digital   signal   processor   comprising   a   bus

3   connectable to a memory; and

4   a   butterfly   coprocessor   [connected]   coupled   to   the

5   [bus,   wherein   the   butterfly   coprocessor]   digital   signal

6   processor to [performs] perform   an   operation   scheduled   by

7   the digital signal processor.

1   2.   The system of claim 1, wherein the digital signal

2   processor further comprises:

3   a data address generator coupled to the bus [, wherein

4   the   data   address   generator]   to   [addresses]   address   the

5   memory on behalf of a requesting device.

1   3.   The system of claim 2, wherein the digital signal

2   processor   further   comprises   an   arithmetic   unit   [for

3   performing] to perform arithmetic operations in the digital

4   signal processor.

1   4.   The   system   of   claim   3,   wherein   the   arithmetic

2   unit   further   comprises   a   branch   metric   unit   [for

3   performing] to perform branch metric calculations.

1   6.   The   system   of   claim   5,   [wherein the data address

2   register   may   address]   further   comprising   one   or   more

3   registers   in   the   arithmetic   unit   addressable   by   the   data

4   address generator.

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1   7.   The system of claim 1, wherein the butterfly
2   coprocessor further includes a plurality of butterfly units
3   [for performing] to perform butterfly operations.

1   9.   The system of claim 8, wherein the plurality of
2   butterfly units in the butterfly coprocessor are coupled to
3   further perform add-compare-select operations at the
4   direction of the digital signal processor.

1   10.   The system of claim 8, wherein the plurality of
2   butterfly units in the butterfly coprocessor are coupled to
3   further perform approximations of [log] logarithmic sum
4   exponential operations at the direction of the digital
5   signal processor.

1   11.   The system of claim 8, wherein the data address
2   generator is coupled to access a path metric retrieved from
3   a path metric memory [is accessed by the data address
4   generator of the digital signal processor].

1   12.   The system of claim 11, wherein the data address
2   generator of the digital signal processor is coupled to
3   [further retrieves] retrieve a branch metric from the
4   branch metric unit.

1   17.   A method comprising:

2   receiving a request to decode a bit stream, wherein
3 the bit stream was encoded by an encoder and the encoder is
4 described using a trellis diagram;
5   [identify] identifying a stage of the trellis diagram;
6   [compute] computing branch metrics for all nodes of
7 the stage;
8   [retrieve] retrieving path metrics for a different
9 stage of the trellis diagram from a memory; and
10   simultaneously [calculate] calculating new path
11 metrics for each node of the stage.

1   18. The method of claim 17, further comprising:
2   storing the new path metrics for each node of the
3 stage in the memory; and
4   [identify] identifying a new stage of the trellis
5 diagram.

1   21. A system comprising:
2   a digital signal processor, comprising:
3   a bus connectable to a memory;
4   a data address generator and
5   an arithmetic unit; and
6   a butterfly coprocessor [connected] coupled to the
7 [bus, wherein the butterfly coprocessor performs] digital
8 signal processor to perform an operation scheduled by the
9 digital signal processor.

1   22. The system of claim 21, wherein the digital
2   signal processor further comprises a software program
3   which, upon execution, causes the system to:
4   [identifies] identify a stage of a trellis diagram;
5   [identifies] identify a number of nodes in the stage;
6   and
7   [identifies] identify a number of branches extending
8   from each node.

1   25. The system of claim 24, wherein [the operation
2   performed by] the butterfly coprocessor is coupled to
3   compute [comprises computing] path metrics for the stage.

1   26. The system of claim 25, wherein the butterfly
2   units are coupled to simultaneously compute a path metric
3   for each node of the stage.